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(71) Applicant:
MITSUBISHI DENKI KABUSHIKI KAISHA
Tokyo 100 (JP)

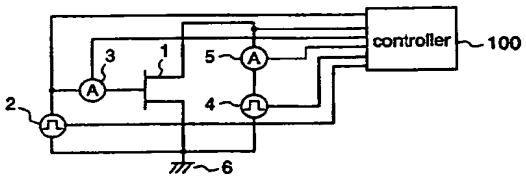
(72) Inventors:
- **Inoue, Akira**
  Chiyoda-ku, Tokyo 100 (JP)
- **Nakajima, Yasuharu**
  Chiyoda-ku, Tokyo 100 (JP)
- **Ohta, Yukio**
  Chiyoda-ku, Tokyo 100 (JP)
- **Matsubayashi, Hiroto**
  Chiyoda-ku, Tokyo 100 (JP)

(74) Representative: **KUHNEN, WACKER & PARTNER**
Alois-Steinecker-Strasse 22
85354 Freising (DE)

(54) Apparatus and method for testing semiconductor element and semiconductor device

(57) An apparatus of testing a semiconductor element (Figs. 1 and 2) includes means for applying pulsed voltages being synchronized with each other, respectively, to a gate and a drain of a semiconductor element (1) as a target of testing, and means for measuring a current flowing through the semiconductor element (1) by the pulsed voltages thus applied. Therefore, it is provided an apparatus of testing a semiconductor element capable of obtaining the pulsed I-V characteristics with considerations of the influences of heat and surface level of a semiconductor element, and a RF swing along a load line in a large signal operation of a high-power output FET.

Fig.1



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Description

FIELD OF THE INVENTION

The present invention relates to an apparatus and a method for testing a semiconductor element utilizing a pulsed I-V measurement system, and a semiconductor device.

BACKGROUND OF THE INVENTION

Figure 36 is a circuit diagram illustrating a prior art I-V measurement circuit as a kind of apparatus for testing a semiconductor element. In the figure, reference numeral 1 designates a semiconductor element such as a GaAs FET and a Si FET, as a target of testing. A source of the semiconductor element 1 is connected to a ground 6 of this measurement circuit. Reference numeral 23 designates a DC power source, and the negative pole of the DC power source 23 is connected to the source of the semiconductor element 1. Reference numeral 30 designates a DC power source, and the negative pole of the DC power source 30 is connected to the source of the semiconductor element 1. Reference numeral 31 designates a current measuring apparatus, such as an ammeter, which is connected between a drain of the semiconductor element 1 and the positive pole of the DC power source 23. Reference numeral 32 designates a current measuring apparatus, such as an ammeter, which is connected between a gate of the semiconductor element 1 and the positive pole of the DC power source 30.

A description is given of the operation.

Bias voltages from the DC power sources 30 and 23 are applied to the gate and the drain of the semiconductor element 1 as a target of testing, respectively. The current flowing through the gate is measured with the current measuring apparatus 32. Then, a change in the drain current flowing through the semiconductor element 1 due to a change in the bias voltage applied to the gate is measured with the current measuring apparatus 31. Consequently, I-V measurements of the target of testing by inputting a continuous wave (hereinafter referred to as CW) are performed.

By measuring I-V characteristics by the CW input, it is possible to measure the current-voltage characteristics of the semiconductor element (FET) in a stable state by heat value that is obtained from the product of current flowing through the semiconductor element, and voltage, i.e., the condition in which the current decreases due to heat generation, and in a state in which electronic charges are stable in a depleted layer in the channel and a surface-depleted layer.

The prior art I-V measurement circuit is arranged as shown in figure 36 and the I-V measurements are performed at the CW input operation, so that the input is continuously applied to this circuit. Therefore, the I-V characteristics are varied because of heat of self-heating, failing to perform the accurate I-V measurements.

In addition, in a recess of such as a GaAs system FET, surface level that adversely affects its characteristics is produced. In the case of a pulse operation, there is a difference between speed of electrons flowing through the channel and speed of electrons at the surface level, whereby the characteristics are varied. In the CW operation, however, since the surface charges are in a stable state, the surface level does not vary, and no influence of the surface level is produced. As a result, the I-V characteristics cannot be measured by considering the influence of the surface level.

Further, it is impossible to obtain the I-V characteristics with consideration of a RF swing along a load line in such a large signal operation of a high-power output FET.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an apparatus and a method for testing a semiconductor element, in which a semiconductor element as a target of testing is set to the operating conditions capable of removing the influence of heat, I-V measurements of the semiconductor element are performed at a desired temperature, the I-V characteristics are measured by considering the influence of surface level in a recess of such as a GaAs system FET, and the I-V characteristics with consideration of a RF swing along a load line in such a large signal operation of a high-power output FET are obtained.

It is another object of the present invention to provide a semiconductor device to which burn-in has been performed by the apparatus and the method for testing a semiconductor element.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the scope of the invention will become apparent to the those skilled in the art from this detailed description.

According to a first aspect of the present invention, an apparatus of testing a semiconductor element includes means for applying pulsed voltages that are synchronized with each other, respectively, to a gate and a drain of a semiconductor element as a target of testing, and means for measuring a current flowing through the semiconductor element by the pulsed voltages applied by the means for applying pulsed voltages. Therefore, it is obtainable an apparatus of testing a semiconductor element which realizes the pulsed I-V characteristics with considerations of the influences of heat in a semiconductor element and of surface level in such as an FET, and a RF swing along a load line in a large signal operation of a high-power output FET.

According to a second aspect of the present invention, a method of testing a semiconductor element includes applying pulsed voltages that are synchronized

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with each other, respectively, to a gate and a drain of a semiconductor element as a target of testing, and measuring a current flowing through the semiconductor element by the applied pulsed voltages. Therefore, it is obtainable a method of testing a semiconductor element which realizes the pulsed I-V characteristics with considerations of the influences of heat in a semiconductor element and of surface level in such as an FET, and a RF swing along a load line in a large signal operation of a high-power output FET.

According to a third aspect of the present invention, load is interposed on the drain side in the semiconductor element testing apparatus of the first aspect of the invention. Therefore, it is obtainable an apparatus of testing a semiconductor element which realizes the pulsed I-V characteristics with considerations of the influences of heat and surface level of an FET, and a RF swing along a load line in a large signal operation of a high-power output FET, when the load is actually interposed.

According to a fourth aspect of the present invention, load is interposed on the drain side in the semiconductor element testing method of the second aspect of the invention. Therefore, it is obtainable a method of testing a semiconductor element which realizes the pulsed I-V characteristics with considerations of the influences of heat in a semiconductor element and of surface level in such as an FET, and a RF swing along a load line in a large signal operation of a high-power output FET, when the load is actually interposed.

According to a fifth aspect of the present invention, the semiconductor element testing method of the second aspect of the invention further includes detecting variation of a drain current flowing through the drain by varying a voltage applied to the gate of the semiconductor element, thereby measuring transconductance gm on a load line. Therefore, it is obtainable a method of testing a semiconductor element which enables to measure transconductance gm on a load line with considerations of the influences of heat and surface level of an FET, and a RF swing along a load line in a large signal operation of a high-power output FET.

According to a sixth aspect of the present invention, the semiconductor element testing method of the second aspect of the invention further includes detecting variation of a drain current flowing through the drain by varying a voltage applied to the gate of the semiconductor element, thereby measuring frequency dispersion of transconductance gm on a load line. Therefore, it is obtainable a method of testing a semiconductor element which enables to measure frequency dispersion of transconductance gm on a load line with considerations of the influences of heat and surface level of an FET, and a RF swing along a load line in a large signal operation of a high-power output FET.

According to a seventh aspect of the present invention, the semiconductor element testing method of the second aspect of the invention further includes detecting variation of a drain current flowing through the drain by varying a voltage applied to the drain of the semiconductor element, thereby measuring drain conductance gd on a load line. Therefore, it is obtainable a method of testing a semiconductor element which enables to measure drain conductance gd on a load line with considerations of the influences of heat and surface level of an FET, and a RF swing along a load line in a large signal operation of a high-power output FET.

According to an eighth aspect of the present invention, the semiconductor element testing method of the second aspect of the invention further includes detecting variation of a drain current flowing through the drain by varying a voltage applied to the drain of the semiconductor element, thereby measuring frequency dispersion of drain conductance gd on a load line. Therefore, it is obtainable a method of testing a semiconductor element which enables to measure frequency dispersion of drain conductance gd on a load line with considerations of the influences of heat and surface level of an FET, and a RF swing along a load line in a large signal operation of a high-power output FET.

According to a ninth aspect of the present invention, a membrane probe is employed in the semiconductor element testing apparatus of the first aspect of the invention. Therefore, on-wafer test is performed with production of a parasitic element suppressed.

According to a tenth aspect of the present invention, in the semiconductor element testing method of the fourth aspect of the invention, there are employed pulses having a positive pulse and a negative pulse that are alternately repeated at regular intervals. Therefore, it is obtainable a method of testing a semiconductor element, by which a test is performed at low cost and with high precision without causing hysteresis.

According to an eleventh aspect of the present invention, in the semiconductor element testing method of the fourth aspect of the invention, there are employed pulses having a positive pulse and a negative pulse produced immediately after the positive pulse n ($n \geq 1$) times, these pulses being repeated at regular intervals. Therefore, it is obtainable a method of testing a semiconductor element, by which a test is performed at low cost and with high precision without causing hysteresis.

According to a twelfth aspect of the present invention, in the semiconductor element testing method of the fourth aspect of the invention, the pulses have a positive pulse and a negative pulse that are alternately repeated. Therefore, it is obtainable a method of testing a semiconductor element, by which a test is performed at low cost and with high precision without causing hysteresis.

According to a thirteenth aspect of the present invention, in the semiconductor element testing method of the fourth aspect of the invention, the pulses include a pulse for discharging an electronic charge immediately before applying a pulse for measurement. Therefore, it is obtainable a method of testing a semiconductor element, by which a test is performed at low cost and with high precision without causing hyster-

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esis.

According to a fourteenth aspect of the present invention, the semiconductor element testing method of the eleventh aspect of the invention further includes measuring I-V characteristics along a load line using the pulses. Therefore, it is obtainable a method of testing a semiconductor element, by which the I-V characteristics along a load line of the element are measured at low cost and with high precision.

According to a fifteenth aspect of the present invention, the semiconductor element testing method of the eleventh aspect of the invention further includes calculating drain conductance gd along a load line by sweeping drain voltage Vd with gate voltage Vg of the respective points of the load line held in a given value. Therefore, it is obtainable a method of testing a semiconductor element, by which drain conductance gd along a load line is calculated at low cost, without causing hysteresis.

According to a sixteenth aspect of the present invention, the semiconductor element testing method of the eleventh aspect of the invention further includes calculating transconductance gm along a load line by sweeping gate voltage Vg with drain voltage Vd of the respective points of the load line held in a given value. Therefore, it is obtainable a method of testing a semiconductor element, by which transconductance gm along a load line is calculated at low cost, without causing hysteresis.

According to a seventeenth aspect of the present invention, the semiconductor element testing method of the fourteenth aspect of the invention further includes calculating resistance dependency of the maximum output power P_{max} by sweeping resistance R of a load line and repeating measurement of I-V characteristics along the load line. Therefore, it is obtainable a method of testing a semiconductor element, by which resistance dependency of the maximum output power P_{max} is calculated at low cost, without causing hysteresis.

According to an eighteenth aspect of the present invention, in an apparatus of testing a semiconductor element, burn-in to a semiconductor element is performed using the semiconductor element testing method of the eleventh aspect of the invention. Therefore, it is obtainable an apparatus of testing a semiconductor element, by which burn-in to a semiconductor element is performed without employing an expensive microwave producing apparatus.

According to a nineteenth aspect of the present invention, in a semiconductor device, burn-in has been performed using the semiconductor element testing method of the eleventh aspect of the invention. Therefore, burn-in is performed without employing an expensive microwave producing apparatus, so that the cost required for the burn-in is prevented from increasing the costs of a semiconductor device, thereby obtaining a low-priced semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram illustrating a principle of an apparatus for testing a semiconductor element in accordance with a first embodiment of the present invention.

Figure 2 is a circuit diagram illustrating a structure of an apparatus for testing a semiconductor element according to the first embodiment of the invention.

Figure 3 is a diagram illustrating a method of determining the conditions in order to remove the influence of heat in the apparatus for testing a semiconductor element according to the first embodiment of the invention.

Figure 4 is a flowchart of a method of testing a semiconductor element in accordance with a second embodiment of the present invention.

Figure 5 is a diagram illustrating the wave shapes of pulses that are applied to the respective parts of a semiconductor element using the method of testing a semiconductor element according to the second embodiment of the invention.

Figure 6 is a graph showing the pulsed I-V characteristics when a semiconductor element is observed according to the second embodiment of the invention.

Figure 7 is a diagram illustrating the pulse waveforms on an oscilloscope when a semiconductor element is observed according to the second embodiment of the invention.

Figure 8 is a diagram showing by comparing the short-pulsed I-V characteristics according to the second embodiment with the prior art I-V characteristics at the CW operation.

Figure 9 is a circuit diagram illustrating a principle of an apparatus for testing a semiconductor element in accordance with a third embodiment of the present invention.

Figure 10 is a circuit diagram illustrating a structure of an apparatus for testing a semiconductor element according to the third embodiment of the invention.

Figure 11 is a flowchart of a method of testing a semiconductor element in accordance with a fourth embodiment of the present invention.

Figure 12 is a diagram illustrating the wave shapes of pulses that are applied to the respective parts of a semiconductor element using the method of testing a semiconductor element according to the fourth embodiment of the invention.

Figure 13 is a graph showing the pulsed I-V characteristics when a semiconductor element is measured using the testing method according to the fourth embodiment of the invention.

Figure 14 is a graph showing a method for testing transconductance gm in accordance with a fifth embodiment of the present invention.

Figure 15 is a diagram illustrating one instance of a membrane probe core in accordance with a sixth embodiment of the present invention.

Figure 16 is a circuit diagram illustrating an equivalent circuit of a measurement system of a testing appa-

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ratus according to the prior art and the sixth embodiment of the invention.

Figure 17 is a diagram showing timings in pulsed I-V measurements according to the prior art testing method.

Figure 18 is a graph showing the results of the I-V characteristics measurements when ΔVd is larger than 0, according to the prior art testing method.

Figure 19 is a graph showing the results of the I-V characteristics measurements when ΔVd is smaller than 0, according to the prior art testing method.

Figure 20 is a process flow of general I-V measurements according to the prior art testing method.

Figure 21 is a diagram showing timings of Vd and Vg when high-frequency signals are applied.

Figure 22 is a diagram showing timings of Vd and Vg in accordance with a seventh embodiment of the present invention.

Figure 23 is a diagram showing another timings of Vd and Vg according to the seventh embodiment of the invention.

Figure 24 is a diagram showing still another timings of Vd and Vg according to the seventh embodiment of the invention.

Figure 25 is a diagram showing further timings of Vd and Vg according to the seventh embodiment of the invention.

Figure 26 is a diagram showing still further timings of Vd and Vg according to the seventh embodiment of the invention.

Figure 27 is a graph showing the results of the I-V characteristics measurements along a load line (Vg is fixed), in accordance with an eighth embodiment of the present invention.

Figure 28 is a process flow of I-V measurements along a load line when Vg is fixed, according to the eighth embodiment of the invention.

Figure 29 is a graph showing the results of Gd measurements along a load line according to the eighth embodiment of the invention.

Figure 30 is a graph showing the results of the I-V characteristics measurements along a load line (Vd is fixed), according to the eighth embodiment of the invention.

Figure 31 is a diagram illustrating simple models of equivalent circuits of an FET, according to the eighth embodiment of the invention.

Figure 32 is a graph showing the results of gm measurements along a load line, according to the eighth embodiment of the invention.

Figure 33 is a process flow of I-V measurements along a load line when Vd is fixed, according to the eighth embodiment of the invention.

Figure 34 is a graph showing the results of the I-V characteristics measurements that are obtained by sweeping load resistance R, according to the eighth embodiment of the invention.

Figure 35 is a graph showing the results of measurements of load resistance dependency of the maximum output power P_{max}, according to the eighth embodiment of the invention.

Figure 36 is a circuit diagram illustrating a principle of an apparatus for testing a semiconductor element according to the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[Embodiment 1]

Figure 1 is a circuit diagram illustrating a principle structure of an apparatus for testing a semiconductor element according to a first embodiment of the present invention. In the figure, reference numeral 1 designates a semiconductor element such as a GaAs FET and a Si FET, as a target of testing. Reference numerals 2 and 4 designate pulse generators that are synchronized with each other and apply pulsed voltages to the gate and the drain of the semiconductor element 1, respectively. These pulse generators can accurately set voltages under the condition of a load impedance of 50 Ω. Reference numerals 3 and 5 designate current measuring apparatuses each for monitoring a current. The current measuring apparatus 3 is connected between the gate of the semiconductor element 1 and one end of the pulse generator 2, and measures the current flowing from the pulse generator 2 to monitor the load impedance of the pulse generator 2, thereby ascertaining whether the pulse generator 2 is accurately generating the voltage that is set. The current measuring apparatus 5 is connected between the drain of the semiconductor element 1 and one end of the pulse generator 4, and measures the drain current of the semiconductor element 1. Reference numeral 6 designates a ground of this testing apparatus, and the source of the semiconductor element 1 and the other ends of the pulse generators 2 and 4 are connected to the ground 6. Reference numeral 100 designates a controller. The controller 100 measures the currents of the current measuring apparatuses 3 and 5, and is synchronized with the pulse generators 2 and 4 to measure the output voltages of the pulse generators 2 and 4.

Figure 2 is a circuit diagram illustrating a structure of an apparatus for testing a semiconductor element according to the first embodiment of the invention. In the figure, reference numeral 7 designates an oscilloscope that measures voltages applied to the semiconductor element 1 and a current flowing through the semiconductor element 1. The oscilloscope may be replaced with another which has current and voltage measuring functions and a controlling function similar to those of the oscilloscope 7. Reference numerals 8a to 8d designate input channels of the oscilloscope 7. The input channel 8a is for inputting a triggering signal that is output from the pulse generator 2 or 4 to the other. The input channels 8b and 8c are for observing the pulsed voltages that are output from the pulse generators 2 and 4, respectively. The input channel 8d is for observing the

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current flowing through the semiconductor element 1.

Reference numeral 9 designates a triggering signal line for synchronizing the pulse generators 2 and 4 and the oscilloscope 7 in point of time. Reference numerals 10a and 10b designate voltage probes for measuring the gate and the drain voltages of the semiconductor element 1, respectively. Reference numeral 11 designates a current probe for measuring the drain current of the semiconductor element 1. Since the pulse generator 2 can accurately generate the voltage that is set, the function corresponding to the current measuring apparatus 3 shown in figure 1 is not shown in figure 2.

A description is given of the operation.

In the apparatus for testing a semiconductor element according to the first embodiment of the invention, one pulse generator 2 (4) produces a triggering signal. The produced signal is input to the other pulse generator 4 (2) and the oscilloscope 7, through the triggering signal line 9. Alternatively, the pulse generators 2 and 4 may receive a triggering signal that is output from the oscilloscope 7. Then, the oscilloscope 7 and the pulse generators 2 and 4 are synchronized with each other, and the pulse generators 2 and 4 generate pulsed voltages and apply the same to the gate and the drain of the semiconductor element (FET) 1, respectively. The oscilloscope 7 is synchronized with the pulse generators 2 and 4 by the triggering signal, and inputs the pulsed voltages output from the pulse generators 2 and 4 through the probes 10a and 10b, respectively. Further, the oscilloscope inputs the drain current flowing through the semiconductor element 1 through the probe 11, and observes the drain current.

Therefore, in the first embodiment of the invention, there can be measured the pulsed I-V characteristics, i.e., the current-voltage characteristics of the semiconductor element (FET) in a transient state of heat value that is obtained from the product of current transiently flowing through the semiconductor element, and voltage, with the influence of a depleted layer in the channel that is produced due to surface charges transiently varying, and in a transient state of electronic charges in a surface-depleted layer.

By setting a semiconductor element (FET) as described below, the operating conditions for removing the influence of heat are determined for the semiconductor element. Specifically, the above conditions are determined by a heat value generated in the semiconductor element (FET), which value is obtained from the product of current and voltage, and the radiation effect of the semiconductor element and the substrate. Therefore, the conditions of FETs are different depending on such as the structures of the FETs. In order to determine the conditions, as shown in figure 3, a gate voltage Vg (drain voltage Vd) having a relatively large pulse width, for example, 1 to 10 ms, is applied to the semiconductor element to measure a drain current Id, whereby the gate voltage Vg (drain voltage Vd) and the drain current Id are set to have a pulse width before the drain current decreases due to heat generation.

Consequently, according to the first embodiment of the invention, in the apparatus of testing a semiconductor element, the pulse generators 2 and 4 are synchronized with each other to apply the pulsed voltages to the semiconductor element, and further, the oscilloscope 7 is synchronized with the pulse generators. Therefore, it is possible to obtain the pulsed I-V characteristics with considerations of the influences of heat and surface level of the semiconductor element, thereby making it possible to distinguish superior elements from inferior ones.

[Embodiment 2]

Figure 4 shows a flowchart of a method of testing a semiconductor element according to a second embodiment of the present invention.

In figure 4, S_1 is a process step for synchronizing and generating a pulsed gate voltage and a pulsed drain voltage, S_2 is a process step for applying the pulsed gate voltage and the pulsed drain voltage thus synchronized and generated to a semiconductor element, S_3 is a process step for measuring a gate voltage, a drain voltage and a drain current of the semiconductor element with an oscilloscope, and S_4 is a process step for plotting the results of the measurements.

Figure 5 shows wave shapes of pulses that are applied to the respective parts of a semiconductor element using the method of testing a semiconductor element according to the second embodiment of the invention.

In figure 5, reference numeral 12 designates a pulsed gate voltage that is applied to the gate of the semiconductor element 1, numeral 13 designates a pulsed drain voltage that is applied to the drain of the semiconductor element 1, and numeral 14 designates a pulsed drain current that flows through the drain of the semiconductor element 1 by applying the pulsed gate voltage 12 and the pulsed drain voltage 13. Reference numerals 15a and 15b designate a pulse width and a pulse period of the pulsed drain current 14, respectively. Reference numerals 16a, 17a and 18a designate a gate voltage, a drain voltage and a drain current respectively, when the semiconductor element 1 is turned on. Reference numerals 16b, 17b and 18b designate a gate voltage, a drain voltage and a drain current respectively, when the semiconductor element 1 is turned off. Reference numerals 19a to 19c designate points of observation when the semiconductor element 1 is turned on, and numerals 19d to 19f designate points of observation when the semiconductor element 1 is turned off.

Figure 6 is a graph showing the pulsed I-V characteristics when a semiconductor element is measured using the testing method of the second embodiment. The ordinate is set from a few mA to 2 A, and the abscissa is set to 0 to 100 V (usually 20 V).

In figure 6, reference numeral 20 designates a pulsed I-V curve. The pulsed I-V curve 20 is obtained by applying the mutually synchronized pulses to the gate

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and the drain of the semiconductor element as a target of measuring, and plotting the I-V characteristics. More specifically, it is observed the drain current 18a at the observation point 19c shown in figure 5, which current is obtained when the values of the gate voltage 16a and the drain voltage 17a at the observation points 19a and 19b are respectively varied, whereby the I-V characteristics are plotted.

The method of testing a semiconductor element according to the second embodiment includes, using the apparatus shown in figure 2, synchronizing the pulsed gate voltage 12 and the pulsed drain voltage 13 with each other, applying them to the semiconductor element 1, thereby observing the drain current 14 flowing through the semiconductor element 1.

A more detailed description is given of the testing method. In the process steps S_1 and S_2 shown in figure 4, the pulse generator 2 generates the pulsed gate voltage (16a, 16b) having the pulse width 15a and the pulse period 15b to apply the same to the gate of the semiconductor element 1. The pulse generator 4 generates the pulsed drain voltage (17a, 17b) having the pulse width 15a and the pulse period 15b, which voltage is synchronized with the pulsed gate voltage (16a, 16b), to apply the same to the drain of the semiconductor element 1. As a result of applying these pulsed voltages, the drain current (18a, 18b) flows through the semiconductor element 1.

In the process step S_3, the oscilloscope 7 is synchronized with the pulse generators 2 and 4, and measures the gate voltage, the drain voltage and the drain current that compose the pulsed I-V curve 20 at the observation points 19a, 19b and 19c, respectively. Further, the oscilloscope 7 measures the gate voltage, the drain voltage and the drain current when the semiconductor element 1 is turned off at the observation points 19d, 19e and 19f, respectively. Finally, in the process step S_4, the results of the measurements are plotted.

Figure 7 shows pulse waveforms on the oscilloscope that are observed using the apparatus and method for testing a semiconductor element (FET), according to the present invention. In figure 7, reference numeral 21 designates a triggering signal for synchronizing the pulse generators 2 and 4. The pulse width 15a is 1 μs, and the pulse period 15b (not shown) is 100 μs. The gate voltage 16a in the ON state is 0 V, and the gate voltage 16b in the OFF state is -3 V. The drain voltage 17a in the ON state is 0.3 V. In addition, the set voltage is larger than 0.3 V because a current flows into the pulse generator 4.

Figure 8 shows, by solid lines 22, the results of measurements of the gate voltage, the drain voltage and the drain current at the observation points 19a, 19b and 19c respectively, when varied the ON-state gate voltage and the ON-state drain voltage as shown in figure 7. The values of the ON-state gate voltage are 0, -0.5, -0.75, -1.0 and -1.5 V in descending order. The values of the ON-state drain voltage are in a range of 0 to 5 V, and the value of the OFF-state drain voltage is 6 V.

In figure 8, the abscissa is in a range of 0 to 5 V (1V/div), and the ordinate is in a range of 0 to 400 mA (50mA/div). Broken lines 21 show the I-V characteristics at the CW operation according to the prior art apparatus shown in figure 36.

As shown in figure 8, the short-pulsed I-V characteristics according to the second embodiment are clearly different from the prior art I-V characteristics at the CW operation. Therefore, it is required to employ the most suitable apparatus and method for testing the I-V characteristics of a semiconductor element (FET), depending on its use and operating conditions.

In the second embodiment of the invention, in order to determine the conditions for removing the influence of heat, as shown in figure 3, a gate voltage Vg (drain voltage Vd) having a relatively large pulse width, for example, 1 to 10 ms, is applied to measure a drain current Id, whereby the gate voltage Vg (drain voltage Vd) and the drain current Id are set to have a pulse width before the drain current decreases due to heat generation.

Consequently, according to the second embodiment of the invention, the method of testing a semiconductor element using the testing apparatus of the first embodiment includes synchronizing the pulsed gate voltage 12 and the pulsed drain voltage 13 with each other and applying the same to the semiconductor element, whereby the pulsed I-V characteristics with considerations of the influences of heat and surface level of the semiconductor element are obtained.

[Embodiment 3]

Figure 9 is a circuit diagram illustrating a principle structure of an apparatus for testing a semiconductor element according to a third embodiment of the present invention. In the figure, reference numeral 1 designates a semiconductor element such as a GaAs FET and a Si FET, as a target of testing. Reference numerals 2 and 4 designate pulse generators that are synchronized with each other and apply pulsed voltages to the semiconductor element 1. One end of the pulse generator 2 is connected to the gate of the semiconductor element 1. Reference numeral 24 designates load such as a resistor, and the load 24 is connected between one end of the pulse generator 4 and the drain of the semiconductor element 1. Reference numeral 6 designates a ground of this testing apparatus, and the source of the semiconductor element 1 and the other ends of the pulse generators 2 and 4 are connected to the ground 6. Reference numeral 100 designates a controller, and the controller 100 is synchronized with the pulse generators 2 and 4 and measures the output voltages of the pulse generators 2 and 4 and the voltages at both ends of the load 24. The apparatus for testing a semiconductor element shown in figure 9 does not have those which correspond to the current measuring apparatuses 3 and 5 shown in figure 1.

Figure 10 is a circuit diagram illustrating a structure

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of an apparatus for testing a semiconductor element according to the third embodiment of the invention. In the figure, reference numeral 7 designates an oscilloscope that measures the voltages applied to the semiconductor element 1 and the current flowing through the semiconductor element 1. The oscilloscope 7 may be replaced with another which has current and voltage measuring functions similar to those of the oscilloscope 7. Reference numerals 8a to 8c and 8e designate input channels of the oscilloscope 7. The input channel 8a is for inputting a triggering signal that is output from the pulse generator 2 or 4 to the other. The input channel 8b is for observing the pulsed voltage that is output from the pulse generator 2. The input channels 8c and 8e are for observing the voltages at both ends of the resistor 24 that is connected to the drain of the semiconductor element 1. Reference numeral 9 designates a triggering signal line for synchronizing the pulse generators 2 and 4 and the oscilloscope 7 in point of time. Reference numeral 10a designates a voltage probe for measuring the gate voltage of the semiconductor element 1, and numerals 10b and 10c designate voltage probes for measuring the voltages at both ends of the resistor 24.

As described above, in the apparatus for testing a semiconductor element according to the third embodiment, the resistor 24 is interposed between the drain of the semiconductor element 1 and the pulse generator 4, and both ends of the resistor 24 are connected to the oscilloscope 7.

A description is given of the operation.

In the apparatus for testing a semiconductor element according to the third embodiment of the invention, one pulse generator 2 (4) produces a triggering signal. The produced signal is input to the other pulse generator 4 (2) and the oscilloscope 7 through the triggering signal line 9. Alternatively, the oscilloscope 7 may produce a triggering signal, which is received by the pulse generators 2 and 4. Thereby, the pulse generators 2 and 4 and the oscilloscope 7 are synchronized with each other. Then, the pulse generators 2 and 4 generate pulsed voltages and apply the same to the gate and the drain of the semiconductor element (FET) 1, respectively. The oscilloscope 7 inputs the pulsed voltage output from the pulse generator 2 through the probe 10a. Further, by applying the pulsed voltage output from the pulse generator 4 to the drain of the semiconductor element 1, a current flows through the drain to produce voltages at both ends of the resistor 24, and the oscilloscope 7 inputs the voltages at both ends of the resistor 24 through the probes 10b and 10c. The potential difference between the both ends is processed in the oscilloscope 7, whereby the drain current flowing through the semiconductor element 1 is observed and the drain voltage of the semiconductor element 1 is also observed.

In the third embodiment of the invention, in order to determine the conditions for removing the influence of heat, as shown in figure 3, a gate voltage Vg (drain voltage Vd) having a relatively large pulse width, for example, 1 to 10 ms, is applied to measure drain current Id, whereby the gate voltage Vg (drain voltage Vd) and the drain current Id are set to have a pulse width before the drain current decreases due to heat generation.

Consequently, according to the third embodiment of the invention, in the apparatus of testing a semiconductor element, the load 24, such as a resistor, is interposed on the drain side of the semiconductor element 1, and the pulsed voltages are applied to the gate and the drain. By applying these pulsed voltages, the voltages are produced at both ends of the load 24, and the pulsed current is measured utilizing the voltages at both ends of the load 24. Therefore, it is possible to obtain the pulsed I-V characteristics with considerations of the influences of heat and surface level of the semiconductor element, and a RF swing along a load line in a large signal operation of a high-power output FET.

In addition, the testing apparatus of the third embodiment may have a pulse generator for driving the gate (drain) only on the gate side (drain side).

[Embodiment 4]

Figure 11 shows a flowchart of a method of testing a semiconductor element according to a fourth embodiment of the present invention.

In figure 11, S_{11} is a process step for synchronizing and generating a pulsed gate voltage and a pulsed drain voltage, S_{12} is a process step for applying the pulsed gate voltage and the pulsed drain voltage thus synchronized and generated to a semiconductor element, S_{13} is a process step for measuring a gate voltage and a drain voltage of the semiconductor element with an oscilloscope, S_{14} is a process step for observing a drain current by measuring voltages at both ends of load with the oscilloscope, and S_{15} is a process step for plotting the results of the measurements.

Figure 12 shows wave shapes of pulses that are applied to the respective parts of a semiconductor element, using the method of testing a semiconductor element according to the fourth embodiment of the invention.

In figure 12, reference numeral 12 designates a pulsed gate voltage that is applied to the gate of the semiconductor element 1, numeral 13 designates a pulsed drain voltage that is applied to the drain of the semiconductor element 1, and numeral 14 designates a pulsed drain current that flows through the drain of the semiconductor element 1 by applying the pulsed gate voltage 12 and the pulsed drain voltage 13. Reference numerals 15a and 15b designate a pulse width and a pulse period of the pulsed drain current 14, respectively. Reference numerals 16a, 26a and 18a designate a gate voltage, a drain voltage and a drain current respectively, when the semiconductor element 1 is turned on. Reference numerals 16b, 26b and 18b designate a gate voltage, a drain voltage and a drain current respectively, when the semiconductor element 1 is turned off. Reference numerals 19a, 19g and 19c designate points of

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observation when the semiconductor element 1 is turned on, and numerals 19d, 19h and 19f designate points of observation when the semiconductor element 1 is turned off.

Figure 13 is a graph showing the pulsed I-V characteristics when a semiconductor element is measured using the testing method according to the fourth embodiment. In figure 13, reference numeral 27 designates a pulsed I-V curve. The pulsed I-V curve 27 is obtained by interposing the resistor on the drain side of the semiconductor element as a target of measuring, applying the pulsed voltages to the gate and the drain of the semiconductor element for their drivings, and plotting the I-V characteristics. Reference numeral 33 designates a load line. In figure 13, the abscissa is in a range of 0 to 5 V (1V/div), and the ordinate is in a range of 0 to 400 mA (50mA/div).

Thus, the method of testing a semiconductor element according to the fourth embodiment includes applying the pulsed gate voltage 12 and the pulsed drain voltage 13 to the semiconductor element 1, measuring the current flowing through the semiconductor element 1 from the potential difference produced at both ends of the resistor 24, and plotting the results of the measurements on the load line 33.

A more detailed description is given of the testing method. In the process steps S_{11} and S_{12}, the pulse generator 2 generates the pulsed gate voltage (16a, 16b) having the pulse width 15a and the pulse period 15b to apply the same to the gate of the semiconductor element 1. The pulse generator 4 generates the pulsed drain voltage (26a, 26b) having the pulse width 15a and the pulse period 15b, which voltage is synchronized with the pulsed gate voltage (16a, 16b), to apply the same to the drain of the semiconductor element 1. As a result of applying these pulsed voltages, the drain current (18a, 18b) flows through the semiconductor element 1.

In the process step S_{13}, the oscilloscope 7 is synchronized with the pulse generators 2 and 4, and measures the gate voltage and the drain voltage that compose the pulsed I-V curve 27 at the observation points 19a and 19g, respectively. Further, the oscilloscope 7 measures the gate voltage and the drain voltage when the semiconductor element 1 is turned off at the observation points 19d and 19h, respectively. In the process step S_{14}, the drain current is observed at the observation points 19c and 19f by the oscilloscope 7. Finally, in the process step S_{15}, the results of the measurements are plotted.

In the fourth embodiment of the invention, in order to determine the conditions for removing the influence of heat, as shown in figure 3, a gate voltage Vg (drain voltage Vd) having a relatively large pulse width, for example, 1 to 10 ms, is applied to measure a drain current Id, whereby the gate voltage Vg (drain voltage Vd) and the drain current Id are set to have a pulse width before the drain current decreases due to heat generation.

Consequently, according to the fourth embodiment of the invention, the method of testing a semiconductor element using the testing apparatus of the third embodiment includes applying the pulsed gate voltage 12 and the pulsed drain voltage 13, thereby obtaining the pulsed I-V characteristics with considerations of the influences of heat and surface level of the semiconductor element, and a RF swing along a load line in a large signal operation of a high-power output FET.

In addition, in the fourth embodiment of the invention, the testing may be performed employing a testing apparatus in which a pulse generator for driving the gate (drain) is provided only on the gate side (drain side).

[Embodiment 5]

Figure 14 is a graph showing a method for testing transconductance gm, using the testing method of the fourth embodiment, according to a fifth embodiment of the present invention.

In the figure, reference numeral 28 designates a formula for calculating transconductance gm, and numeral 29 designates a gm plot that is obtained by interposing a resistor on the drain side of a semiconductor element, applying the pulsed voltages to the gate and the drain, and measuring the current flowing through the drain. In figure 14, the abscissa is in a range of 0 to 5 V (1V/div), and the ordinate is in a range of 0 to 400 mA (50mA/div). Although the gm plot curves in the fifth embodiment, it does not always curve as shown in figure 14, depending on FET characteristics.

The transconductance gm according to the fifth embodiment is calculated by $gm = \Delta Id/\Delta Vg$ when the ON-state gate voltage 16a is varied by $\pm \Delta Vg/2$, and the variation of the drain current flowing then is ΔId, whereby the transconductance gm on the load line 33 is plotted.

Consequently, the method for testing the transconductance gm using the testing method of the fourth embodiment is described in the fifth embodiment of the invention. Therefore, it is obtainable the gm characteristics by the pulsed I-V measurement method taking into account the influences of heat and surface level of the semiconductor element, and a RF swing along a load line in a large signal operation of a high-power output FET.

More specifically, a simulation, with transconductance gm and the influences of heat and surface level close to those in the actual RF operation, is performed.

In this fifth embodiment of the invention, the transconductance gm is calculated by arbitrarily varying periods of measurement, using the testing method according to the fourth embodiment, and its frequency characteristics are plotted, whereby frequency dispersion of the transconductance gm along the load line is obtained.

When the transconductance gm at high frequency is satisfactory, other characteristics of the semiconductor element (FET) are also satisfactory. Therefore, by

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measuring the transconductance gm, the quality of other characteristics of the semiconductor element is indirectly checked.

In addition, the drain conductance gd is plotted along the load line, using the testing method of the fourth embodiment.

More specifically, the drain conductance gd is calculated by gd = $\Delta Id/\Delta Vd$ when the ON-state drain voltage 26a is varied by $\pm \Delta Vd/2$, and variation of the drain current flowing then is ΔId, whereby the drain conductance gd on the load line 33 is plotted.

When the drain conductance gd at high frequency is satisfactory, other characteristics of the semiconductor element (FET) are also satisfactory. Therefore, by measuring the drain conductance gd, other characteristics of the semiconductor element are indirectly checked.

The drain conductance gd is calculated by arbitrarily varying periods of measurement using the testing method according to the fourth embodiment, and its frequency characteristics are plotted, whereby frequency dispersion of the drain conductance gd along the load line is obtained.

When the drain conductance gd along the load line is satisfactory, other characteristics of the semiconductor element (FET) are also satisfactory. Therefore, by measuring the drain conductance gd, other characteristics of the semiconductor element are indirectly checked.

In addition, in the fifth embodiment of the invention, the testing may be performed employing a testing apparatus having a pulse generator for driving the gate (drain) only on the gate side (drain side).

In addition, using the testing apparatus of the first embodiment and the testing method of the second embodiment, the transconductance gm, the drain conductance gd, the frequency dispersion of the transconductance gm and the drain conductance gd are obtained.

Specifically, the testing apparatus of the first embodiment may be used for the testing apparatus used in the testing method according to the fifth embodiment of the invention. The testing method of the second embodiment may be used for the testing method according to the fifth embodiment of the invention.

[Embodiment 6]

Using the first to fifth embodiments of the invention, patterning is performed on a membrane probe, i.e., a kind of probe cards employing a membrane as a flexible material, to constitute a circuit, thereby performing an on-wafer test.

Since this membrane probe is easy to process in capacity and resistance, the on-wafer test is performed without making extra parasitic resistance.

Figure 15 is a diagram illustrating one instance of a membrane probe core according to a sixth embodiment of the invention. In the figure, reference numeral 200 designates an edge sensor needle, numeral 201 designates an optical window for ascertaining with an eye where in the wafer bumps of the membrane probe are making contact with, numeral 202 designates a probe frame, numeral 203 designates a probe board corresponding to a probe substrate, numeral 204 designates a coaxial cable for supplying RF signals, numeral 205 designates a plunger for gaining a width for bumps and fixing the bumps, numeral 206 designates a nickel bump serving as a probe needle, numeral 207 designates a membrane as a flexible material, numeral 208 designates a chip cap (optical), numeral 209 designates a spring for giving elasticity, and numeral 210 designates a mounting screw.

Generally, it is thought that large signal characteristics of a semiconductor device, such as an FET and an HBT, is revealed to a considerable extent by the I-V characteristics of an element. Therefore, there is a method of distinguishing an element by measuring the I-V characteristics of the element. However, in a semiconductor device that is employed at frequencies not less than several hundreds MHz, because various traps due to impurities and lattice stress cause delay, it is required to perform measurements at short-pulses having a pulse width of not more than several hundreds μsec.

These measurements are performed with an apparatus as shown in figure 16. Figure 16 is a circuit diagram illustrating an equivalent circuit of a measurement system of a testing apparatus according to the sixth embodiment of the invention. The structure of the apparatus shown in figure 16 is the same as that shown in figure 1. In the figure, reference numeral 1 designates a semiconductor element, such as an FET and an HBT, and in this case, an FET is employed as the element. Reference numerals 3 and 5 designate ammeters, and numerals 2 and 4 designate pulse generators that generate pulses. At the timings shown in figure 17, Vd_0 and Vg_0 are respectively applied to the drain and the gate of the FET 1, except for periods corresponding to the pulse width, and the pulsed voltages Vd and Vg are respectively applied for periods corresponding to the pulse width, thereby measuring the currents Id and Ig. In addition, the pulse width is 100 ns, Vd is in a range of 10 to 20 V, Vg is 5 V, Id is in a range of several tens mA to 20 A, and Ig is a few mA.

Reference numeral 100 designates a controller, and the controller 100 measures the currents of the ammeters 3 and 5. Further, the controller is synchronized with the pulse generators 2 and 4 and measures the output voltages of the pulse generators 2 and 4.

Figure 20 shows a process flow of the measurement. Initially, the pulsed voltage Vg is set (step S_{31}) and the pulsed voltage Vd is set (step S_{32}). In the process step S_{33}, the pulsed voltages are applied to measure the currents Id and Ig. In the process steps S_{34} and S_{35}, the measurements are repeated by varying Vd by ΔVd until the Vd becomes Vd_{stop}. In the process steps S_{36} and S_{37}, the measurements are repeated by varying Vg by ΔVg until the Vg becomes Vg_{stop}.

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Figure 18 is a graph showing the results of the measurements when ΔVd is 1 V, ΔVg is -1 V, Vd_{stop} is 8 V, Vg_{stop} is -3 V, and Id is in a range of several tens mA to 20 A. Generally, in a semiconductor device having various traps, electrons and holes at the respective traps are captured and released at the respective time constants. Therefore, the states of the traps are affected by the order of the I-V measurements, whereby the results of the measurements are different. This phenomenon is called "hysteresis" because the measured values differ according to the measurement paths.

An example of the hysteresis is described. Figure 19 is a graph showing the results of measurements when ΔVd is -1 V, ΔVg is -1 V, Vd_{stop} is -1 V, Vg_{stop} is -3 V, and Id is in a range of 20 A to several tens mA. In this case, Vd is applied through the reverse path of that shown in figure 18, so that the results of the I-V measurements are different from those shown in figure 18.

When an FET actually operates at high frequency, as shown in figure 21, signals that are obtained by adding sinusoidal waves having amplitudes AVd and AVg to the drain voltage Vd_0 and the gate voltage Vg_0, as bias levels of the FET, respectively, are applied. Therefore, due to the signals of $Vd_0 \pm$ AVd, and $Vg_0 \pm$ AVg, capture and release of electrons and holes at the respective traps are repeated, resulting in a stationary state. Consequently, the I-V measurements causing the hysteresis are different from measurements at the actual high-frequency operation, so that the I-V measurements cannot be used for the element distinction. In addition, in figure 21, one sinusoidal wave is 1 to 0.1 ns, Vd is 20 to 10 V, and Vg is 5 V.

Further, since the I-V characteristics of the element obtained by the above pulsed I-V measurements do not always correlate with the large signal characteristics of the element, a test of inputting high-frequency signals must be performed, so that testing cost increases, resulting in an expensive semiconductor device.

In addition, a burn-in test of a semiconductor device is usually performed by applying high-frequency signals, thus increasing the cost of an apparatus for the burn-in test. Accordingly, a semiconductor device to which the burn-in has been performed also increases the cost.

A semiconductor device in which the costs of an apparatus and a method of testing a semiconductor element causing no hysteresis, and the cost of a burn-in test are reduced, thereby preventing the cost increases, is described in the following embodiments.

[Embodiment 7]

In order to realize measurements causing no hysteresis as described above, the high-frequency signals as shown in figure 21 should be directly applied to a semiconductor element to measure current and voltage waveforms. However, the cost of an apparatus increases as frequency is higher, and it is difficult to sufficiently keep measurement precision. Therefore, by applying pulses each having a pulse width from several hundreds μsec to several hundreds nsec as shown in figure 22, and performing I-V measurements, it is possible to perform the same measurements as in the actual operation shown in figure 21.

More specifically, by adding pulses of ± AVd and ± AVg respectively to the drain voltage Vd_0 and the gate voltage Vg_0, as bias voltages of the FET, that is, by adding pulses of + AVd, - AVd, + AVd, - AVd, • • •, i.e., positive and negative pulses that are alternately repeated, to the drain voltage Vd_0, and adding pulses of - AVg, + AVg, - AVg, + AVg, • • •, i.e., pulses that have a phase opposite to the phase of the pulses added to the drain voltage, to the gate voltage Vg_0, the electric field is applied alternately to the bias points similarly when the sinusoidal waves shown in figure 21 are applied. Therefore, capture and release of electrons and holes at the respective traps occur as in the actual operation, whereby the I-V characteristics equivalent to those in the actual operation are measured.

Strictly speaking, the time constant of the electric field applied to each trap is longer than the time constant at the actual operation. More specifically, in 1 GHz operation, the time constant at a half-wave is 500 psec, while the time constant at a pulse width that is measured is longer, i.e., 100 nsec. It is known that the shortest time constants of the respective levels of various semiconductors, such as compound semiconductors, are generally an order of 100 nsec. Consequently, even when measurements are performed at pulses each having the time constant shorter than 100 nsec, the effect on the traps is not different from that in the time constant of 100 nsec, so that measurements equivalent to those in the actual operation are possible.

In addition, in figure 22, after a pulse having positive (negative) polarity is added to the bias voltage of the FET, a pulse having negative (positive) polarity is added at a regular interval, and the same operation is repeated. As shown in figure 23, however, a pulse having negative (positive) polarity is added immediately after a pulse having positive (negative) polarity is added to the bias voltage of the FET, and the same operation is repeated at regular intervals. As a result, the same effect as shown in figure 22 is obtained.

As shown in figure 24, the operation of producing a negative (positive) pulse immediately after producing a positive (negative) pulse having a pulse width pw may be repeated n times, followed by repeating the above-mentioned operation at regular intervals. Thereby, frequency dispersion of the pulses is suppressed and data are measured many times in a fixed measuring time, so that measurement precision is improved.

Figure 25 shows timings in the case where n shown in figure 24 is infinite. By these timings, the maximum time of measurements per unit time is obtainable, and frequency dispersion is reduced to a minimum. Generally, there is required time for charging a capacitor for pulse output of a pulse generator. Accordingly, it is difficult to define that n is infinite in the measurement in

which Id is large. Consequently, the timings shown in figure 24 in which n is finite are selected in practice, depending on Id.

In addition, in figures 21, 22, 23, 24 and 25, the pulse width is 100 ns, Vd is in a range of 20 to 10 V, Vg is 5 V, Id is in a range of 20 A to several tens mA, and Ig is a few mA.

Although short-pulses are used in the seventh embodiment of the invention, other type pulses, such as sinusoidal waves and Gaussian waves, may be employed. In the case of the sinusoidal waves, it is difficult to produce pulses and to control measurement timing. However, there is the advantage that frequency dispersion is suppressed. In this regard, it is preferable to employ sinusoidal waves.

As described above, according to the seventh embodiment of the invention, the voltages that are obtained by superposing the positive and negative pulses on the bias voltages are applied to the semiconductor element as a target of measurement. Therefore, the I-V characteristics corresponding to those in the actual operation are measured without causing hysteresis. Further, because of the low-frequency pulses, it is possible to fabricate the apparatus at low cost, to perform accurate and high-speed measurements, and to suppress the frequency dispersion of the pulses.

In accordance with timings shown in figure 26, by applying charge-up pulses having large amplitude and negative polarity, before applying pulses for measurement, it is possible to conduct charge-up, by which it is obtained a condition in which every trap is completely captured and released during a measurement cycle. In addition, in figure 26, the charge-up pulse 124 is, for example, -3 V to -5 V, the pulse width is 100 ns, Vd is in a range of 20 to 10 V, Vg is 5 V, Id is in a range of 20 A to several tens mA, and Ig is a few mA.

Consequently, according to the seventh embodiment of the invention, the respective traps are always in a steady state by adding the charge-up pulses. Therefore, the I-V characteristics corresponding to those in the actual operation are accurately measured without causing hysteresis. Further, because of the low-frequency pulses, the apparatus can be fabricated at low cost, leading to accurate and high-speed measurements.

[Embodiment 8]

Figure 27 is a graph showing the results when I-V measurements are performed along a load line 125. The load line of load resistance R has a relation of

$$Vd - Vd_0 = -(Id - Id_0)\,R$$

and this is a load line when load having resistance R is provided on the output side of an FET. Reference numeral 126 designates a Q point, and the Q point is a bias applying point (drain voltage Vd_0, gate voltage Vg_0). In the measurements, the amplitude of Vg are set to 0, 0.5 and 1.0 V, with the Q point at the center. In figure 27, Vd is in a range of 20 to 10 V, and Id is in a range of 20 A to several tens mA.

Figure 28 shows a process flow of the measurement. Initially, in the process steps S_{41}, S_{42} and S_{43}, pulses as shown in figures 22 to 26 are applied to the Q points ($AVd = AVg = 0$) to measure Id and Ig. Then, in the process steps S_{44} and S_{45}, putting AVg = 0.5 V, Vd ($Vd = Vd_0 \neq AVd$) is determined to satisfy $Vd - Vd_0 = -R(Id - Id_0)$. That is, in figure 27, the value of Vd is swept to obtain intersection points of the load line 125 and the I-V curves of $Vg \pm 0.5$ (V), thereby obtaining values of Vd. In the process step S_{46}, it is ascertained whether AVg is larger than AVg_{stop}. The same operation as described above is performed in the case of AVg = 1.0 V.

Since the value of Vd is swept, drain conductance gd at the respective points on the load line 125 is easily calculated by

$$gd = \Delta Id / \Delta Vd$$

whereby the drain conductance gd along the load line is easily obtained as shown in figure 29. In addition, in figure 29, gd is in a range of 0.01 to 0.1, and Vd is in a range of 20 to 10 V.

As described above, in the eighth embodiment of the invention, with the positive and negative pulses having amplitude with respect to the Q points, Id and Vd at the respective points along the load line are measured by sweeping Vd under the condition that Vg is fixed. Therefore, the drain conductance gd along the load line equivalent to that in the actual operation is measured without causing hysteresis. Further, since only portions along the load line are measured, the measured points are fewer than those shown in figures 18 and 19, whereby high-speed measurements are possible.

By obtaining the data of Id and Vd along the load line 125, input and output characteristics of a semiconductor element having load resistance R are obtained by calculation. More specifically, with simple models of equivalent circuits having input resistance Ri as shown in figure 31,

$$Vg = Vg_0 + AVg\sin\omega t$$

$$\text{Input power } P_{in} = (Vg^2 / Ri)\,dt$$

$$\text{Output power } P_{out} = I^2\,dRdt$$

Average drain current at high-frequency

$$\text{input } Id_{RF} = Iddt$$

are obtained.

In figure 31, $AVg\sin\omega t$ represents an alternating-current component of the gate voltage that is input, C1 represents equivalent capacity, L1 represents equivalent inductance, $+ Vg_0$ and $+ Vd_0$ represent bias

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sources, Rg represents a gate resistor, Id (Vg, Vd) represents an equivalent current source, and R represents a load resistor.

From the aforesaid calculation, the maximum output power at the load R P_{max} and P_{2dB}, power added efficiency PAE, drain efficiency E_D, etc. are given.

Although the models shown in figure 31 are used as a model of an FET, other models may be employed.

Consequently, according to the eighth embodiment of the invention, the voltages that are obtained by superposing the positive and negative pulses to the bias voltages are applied to the semiconductor element as a target of measurement. Therefore, the I-V characteristics corresponding to those in the actual operation are measured without causing hysteresis. Further, because of the low-frequency pulses, it is possible to fabricate an apparatus at low cost, to perform accurate and high-speed measurements, and to measure gd and gm along a load line.

In addition, in the eighth embodiment of the invention, although the I-V characteristics along the load line by fixing Vg and sweeping Vd are measured, there is a method of fixing Vd and sweeping Vg as shown in figure 30. In this case, gm at the respective points is easily calculated by

$$gm = \Delta Id / \Delta Vg$$

whereby gm along the load line is easily indicated as shown in figure 32. In addition, in figure 32, gm is in a range of 0.1 to several tens, and Vd is in a range of 20 to 10 V.

Figure 33 shows a process flow of the measurement. Initially, in the process steps S_{51}, S_{52} and S_{53}, pulses as shown in figures 22 to 26 are applied to the Q points (AVd = AVg = 0) to measure Id and Ig. Then, in the process steps S_{54} and S_{55}, putting AVd = 0.5 V, Vd ($Vd = Vd_0 \neq AVd$) is determined to satisfy $Vd - Vd_0 = - R (Id - Id_0)$. That is, in figure 30, the value of Vg is swept to obtain intersection points of the load line 125 and the I-V curves of Vg ± 0.5 (V), thereby obtaining values of Vg. In the process step S_{56}, it is ascertained whether AVd is larger than AVd_{stop}. The same operation as described above is performed in the case of AVd = 1.0 V.

Consequently, according to the eighth embodiment of the invention, with the positive and negative pulses having amplitude with respect to the Q points, Id and Vd at the respective points along the load line are measured by sweeping Vg under the condition that Vd is fixed. Therefore, gm along a load line equivalent to that in the actual operation is measured without causing hysteresis. Further, it is possible to fabricate an apparatus at low cost, to perform accurate and high-speed measurements, and to calculate P_{max} and P_{2dB} to obtain their load dependencies.

Furthermore, as shown in figure 34, the I-V characteristics along the load line are measured by sweeping the values of load resistance R, whereby R dependency of the maximum output power P_{max} and R dependencies of PAE and P_{2dB} are measured and indicated as shown in figure 35.

In figure 34, Vd is in a range of 20 to 10 V, and Id is in a range of 20 A to several tens mA. In figure 35, R is in a range of 0 to 500 Ω (or 1 kΩ), and P_{max} is in a range of 0.1 to 100 W.

Consequently, according to the eighth embodiment of the invention, dependencies of P_{max}, PAE and P_{2dB} on load resistance R, equivalent to those in the actual operation, can be obtained without causing hysteresis, load dependency of a semiconductor element to be measured can be found without applying high-frequency signals, and high-frequency characteristics of the element can be judged at low cost and at high speed to distinguish the element.

[Embodiment 9]

In a ninth embodiment of the present invention, it is obtainable a testing apparatus that can perform the testing methods according to the seventh and eighth embodiments of the invention, with a software in which the testing methods according to the seventh and eighth embodiments are programed.

An apparatus as shown in figure 16 can be exemplified as a hardware of this testing apparatus. In this apparatus, the respective processes as previously described are carried out with the software, whereby element characteristics equivalent to those in the actual operation are easily measured with low-frequency pulses at low cost, at high speed and with high precision, without causing hysteresis.

[Embodiment 10]

By the hardware shown in figure 16, a burn-in apparatus performing burn-in to a semiconductor element by applying pulses as shown in figures 22 to 26, and a burn-in method are obtained, whereby an apparatus of testing a semiconductor element to which the burn-in is performed, and a semiconductor device to which the burn-in has been performed are obtained at low cost.

Generally, in a semiconductor device, various levels (traps) due to impurities and lattice stress are present. Therefore, when a current flows for a long time, the levels increase and decrease, so that element characteristics vary. For this reason, there is employed a burn-in method in which a current is sent in advance to apply electric field stress in order to prevent the variation of the element characteristics. Because much time is spent to simply send DC in a high-frequency element, there is employed a RF burn-in method in which high-frequency signals (continuous wave) are applied in order to prevent the aforesaid variation. However, an apparatus to which high-frequency signals are applied is generally expensive, causing the cost increase of a semiconductor device. Therefore, in place of the high-frequency signals, low-frequency pulses as shown in

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figures 22 to 26 are applied, whereby burn-in is performed at low cost.

Since the time constants of the respective levels are longer than several hundreds nsec as described above, by applying the low-frequency pulses, the electric field stress equivalent to that in the case of applying of the high-frequency signals can be applied, so that the same effects as in the high-frequency signals are obtained. As a result, burn-in is performed with an apparatus of testing a semiconductor element at lower cost than in the prior art RF burn-in, thereby preventing the burn-in cost from increasing the cost of a semiconductor device, leading to its cost decrease.

Claims

1. An apparatus of testing a semiconductor element (Figs. 1 and 2) including:

   means for applying pulsed voltages being synchronized with each other, respectively, to a gate and a drain of a semiconductor element (1) as a target of testing; and
   means for measuring a current flowing through the semiconductor element (1) by the pulsed voltages thus applied.

2. A method of testing a semiconductor element (Fig. 4) including:

   preparing a semiconductor element (1) as a target of testing;
   applying pulsed voltages being synchronized with each other, respectively, to a gate and a drain of the semiconductor element (1) as a target of testing; and
   measuring a current flowing through the semiconductor element (1) by the pulsed voltages thus applied.

3. The apparatus of testing a semiconductor element (Figs. 9 and 10) of claim 1 wherein load (24) is interposed on the drain side of the semiconductor element (1).

4. The method of testing a semiconductor element (Fig. 11) of claim 2 wherein load (24) is interposed on the drain side of the semiconductor element (1).

5. The apparatus of testing a semiconductor element (Fig. 15) of claim 1 wherein a membrane probe is employed.

6. The method of testing a semiconductor element (Fig. 22) of claim 4 wherein the pulses have a positive pulse and a negative pulse that are alternately repeated at regular intervals.

7. The method of testing a semiconductor element (Fig. 24) of claim 4 wherein the pulses have a positive pulse and a negative pulse produced immediately after the positive pulse n ($n \geq 1$) times, the above pulses being repeated at regular intervals.

8. The method of testing a semiconductor element (Fig. 25) of claim 4 wherein the pulses have a positive pulse and a negative pulse that are alternately repeated.

9. The method of testing a semiconductor element (Fig. 26) of claim 4 wherein the pulses include a pulse for discharging an electronic charge immediately before applying a pulse for measurement.

10. A semiconductor device to which burn-in has been performed using the testing method of claim 7.

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Fig.1

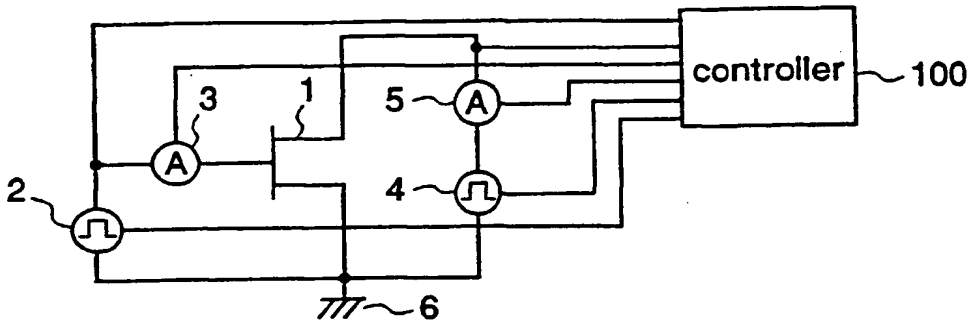

Fig.2

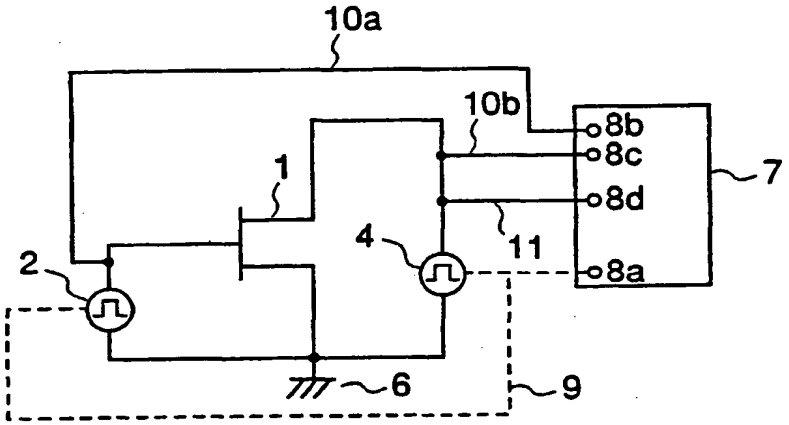

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Fig.3

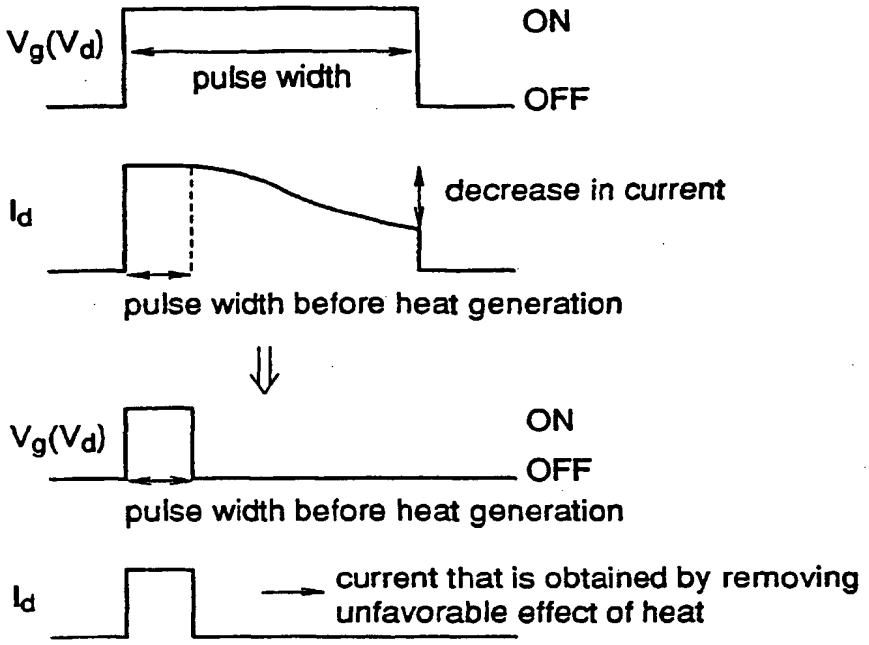
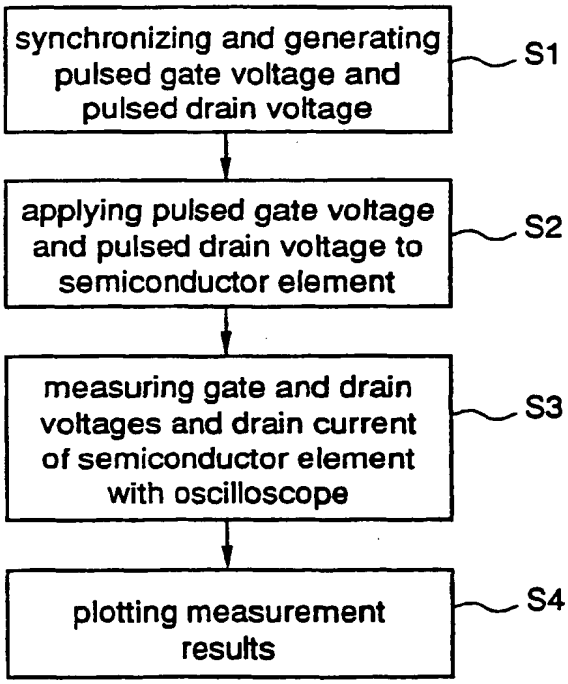


Fig.4



ID: <EP 0800091A2 I >

Fig.5

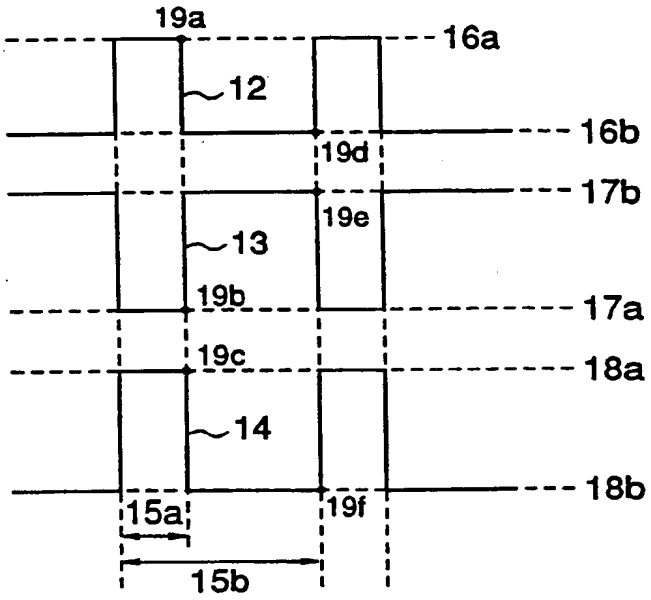
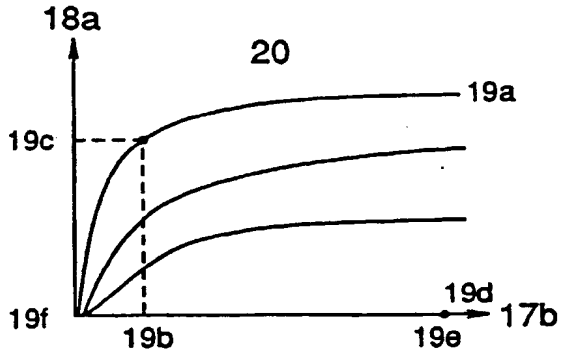


Fig.6



ID: <EP 0800091A2 I >

Fig.7

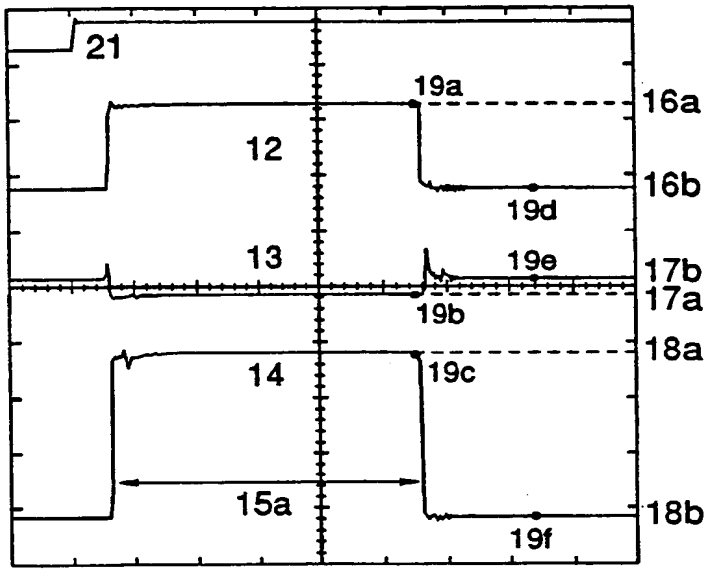
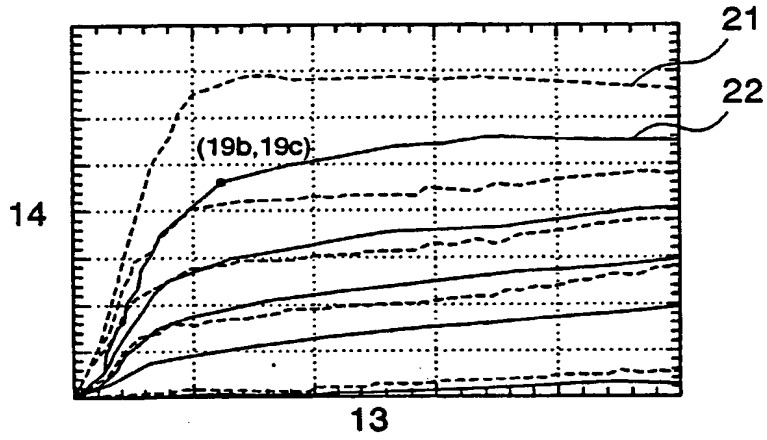


Fig.8



CID: <EP 0800091A2 I >

Fig.9

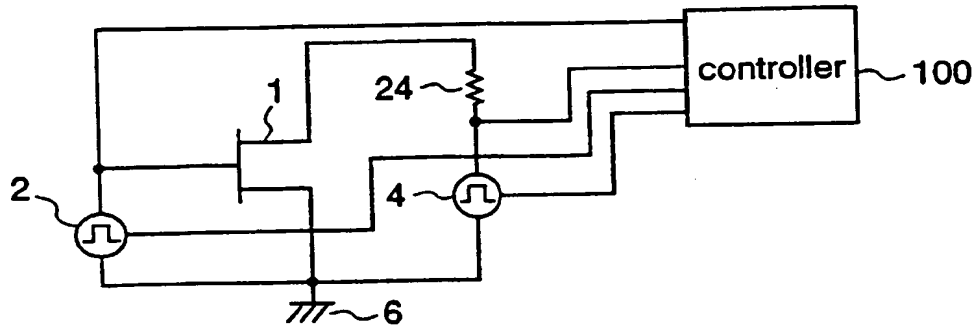


Fig.10

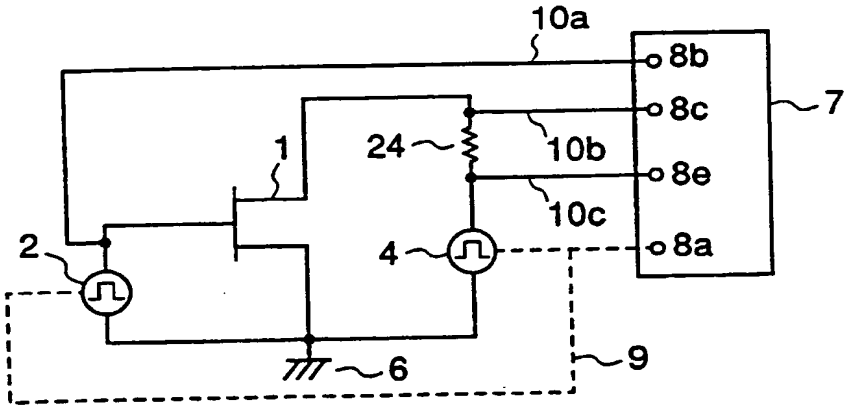


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Fig.11

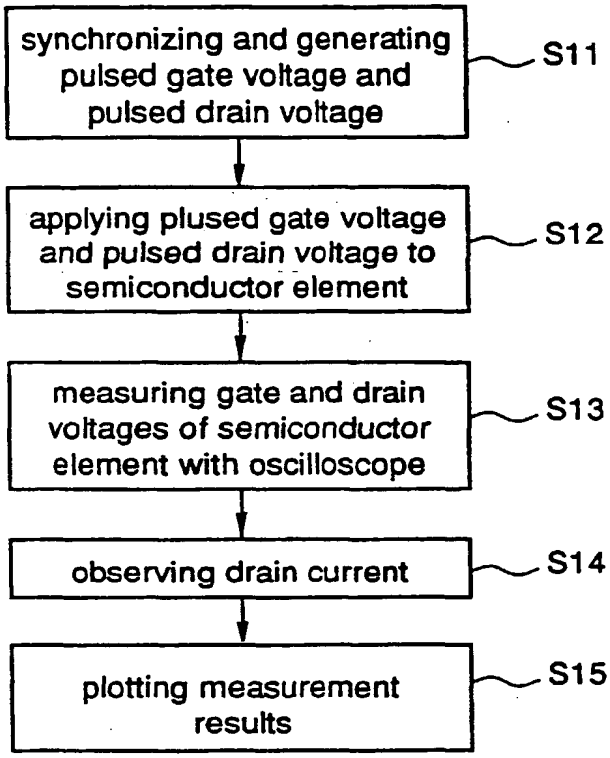
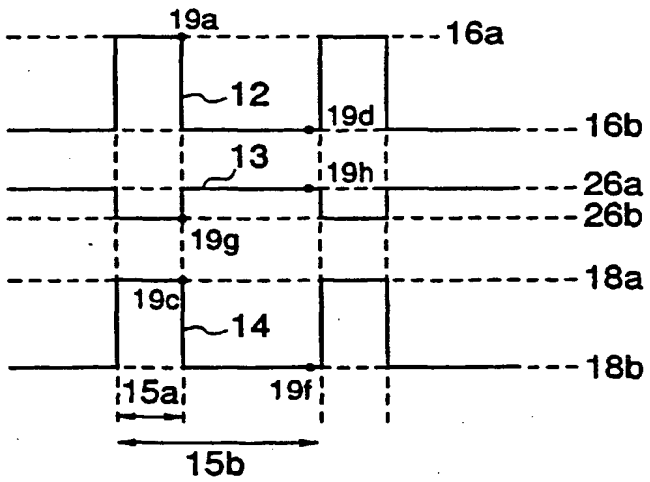


Fig.12



EPO <EP 0800091A2 I >

Fig.13

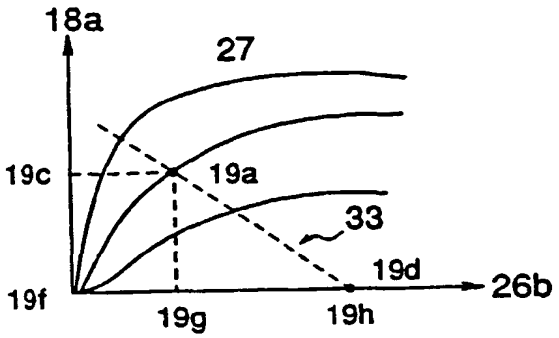
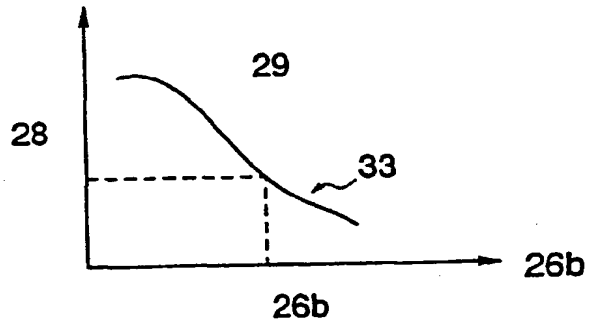


Fig.14



ID: <EP 0800091A2 I >

Fig.15

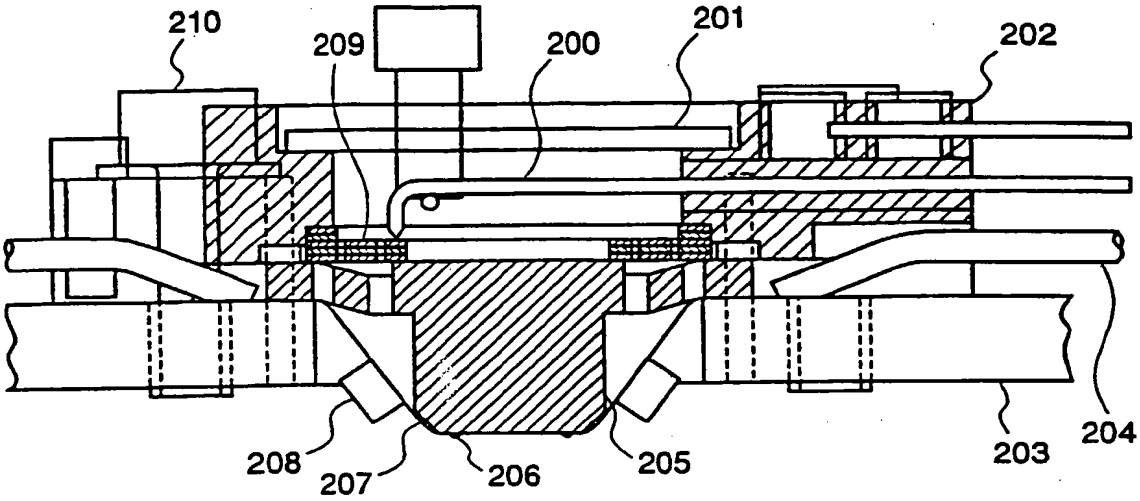


Fig.16

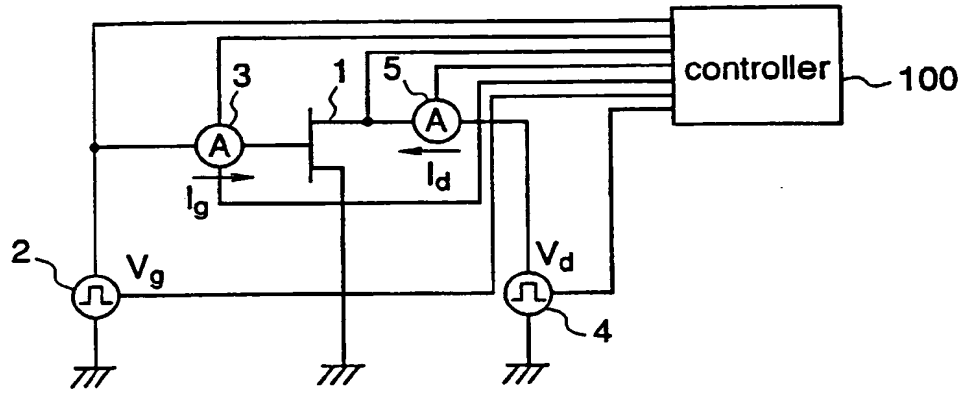


Fig.17

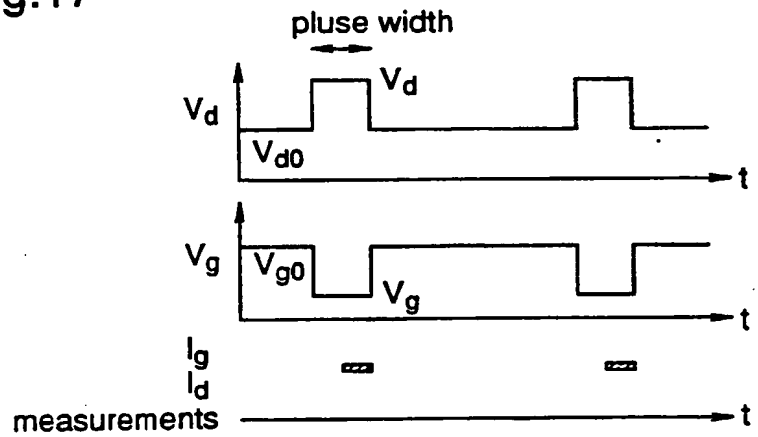


Fig.18

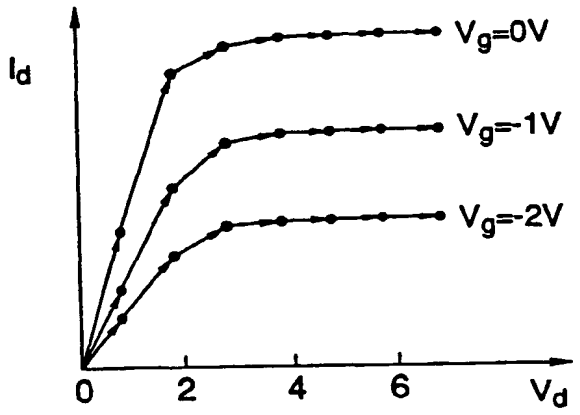


Fig.19

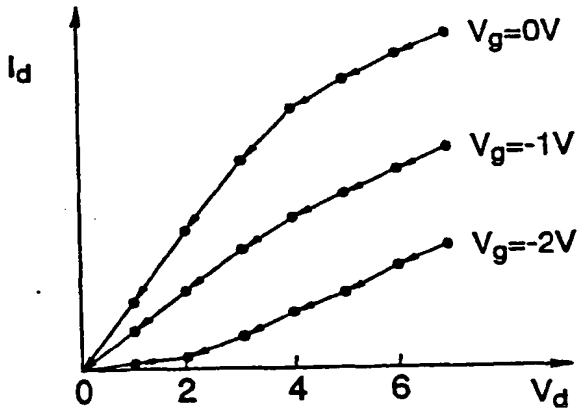


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Fig.20

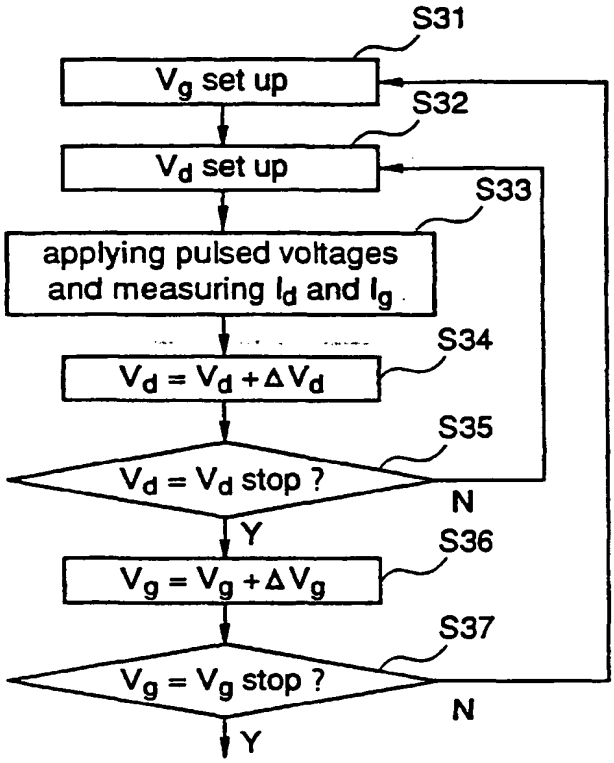

Fig.21

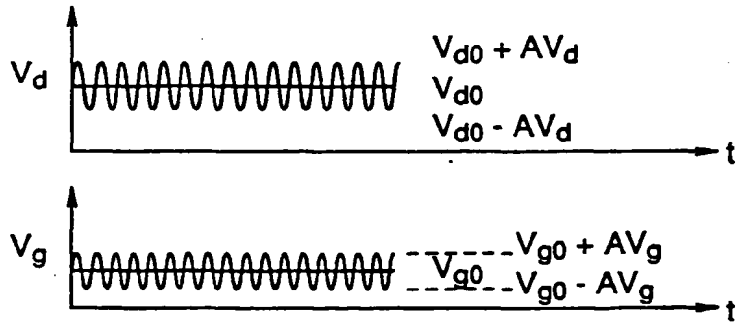

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Fig.22

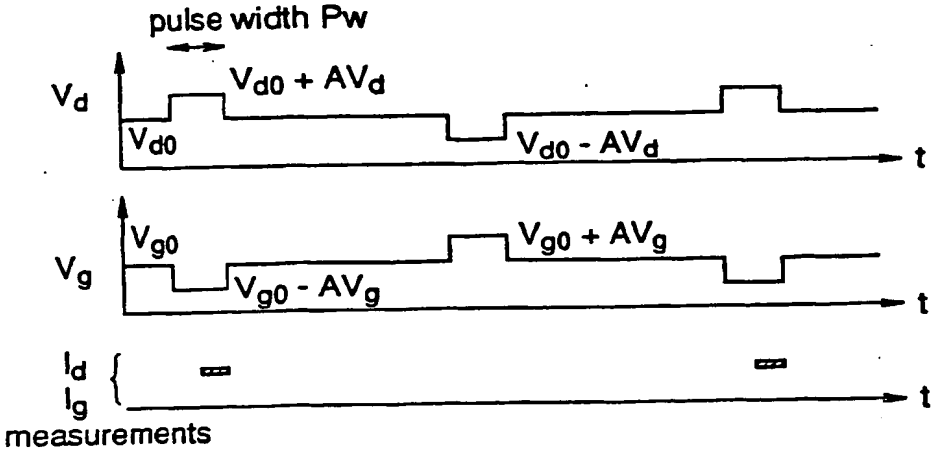


Fig.23

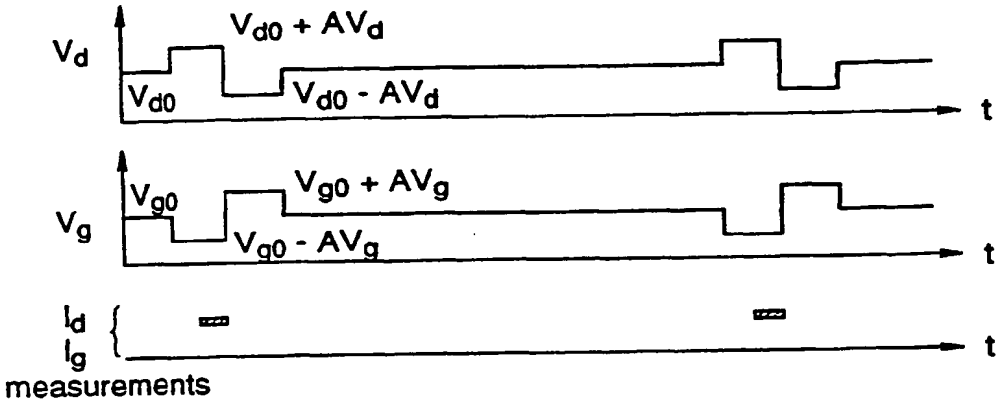


Fig.24

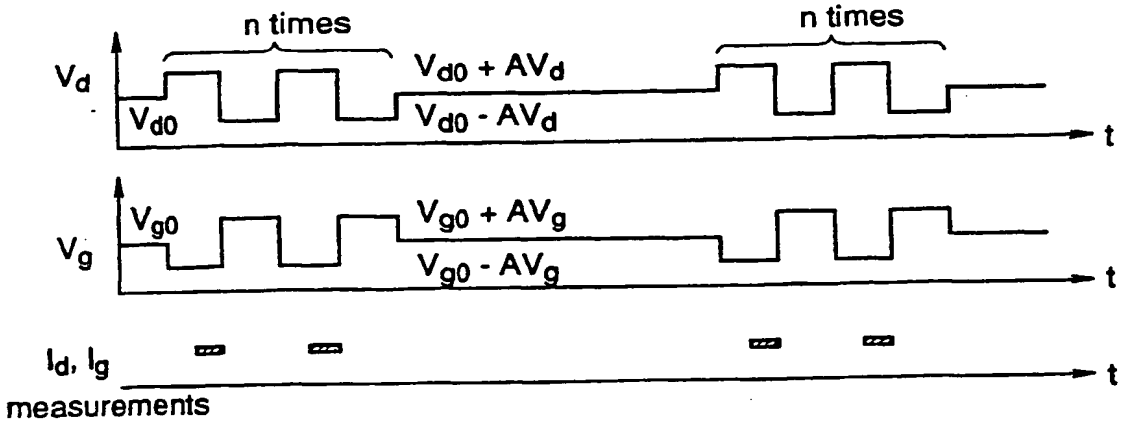
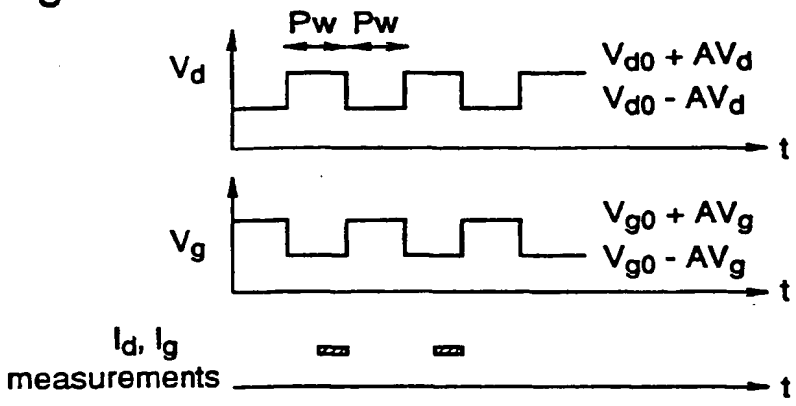


Fig.25



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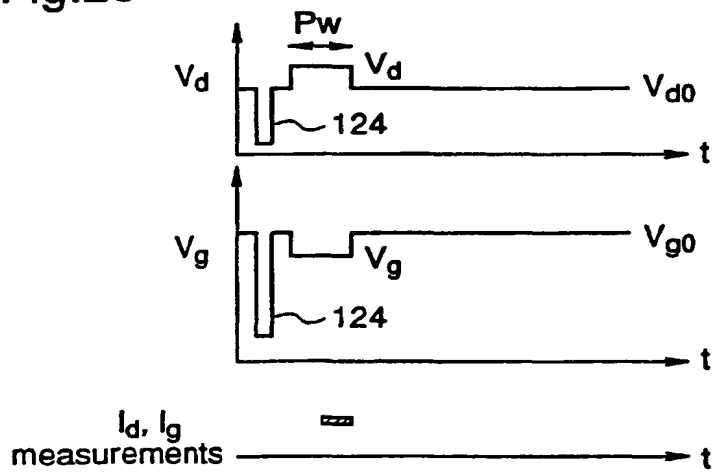

Fig.27

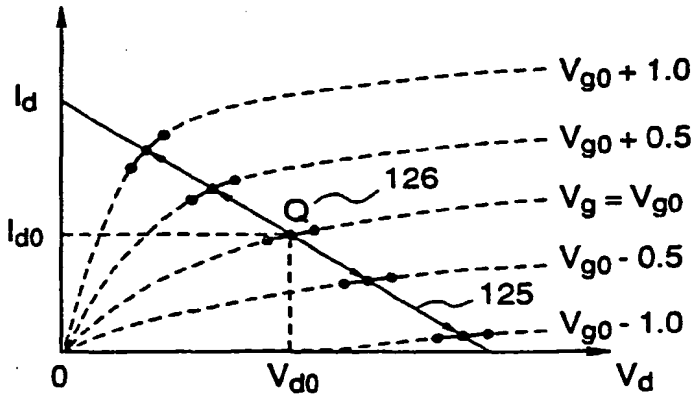

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Fig.28

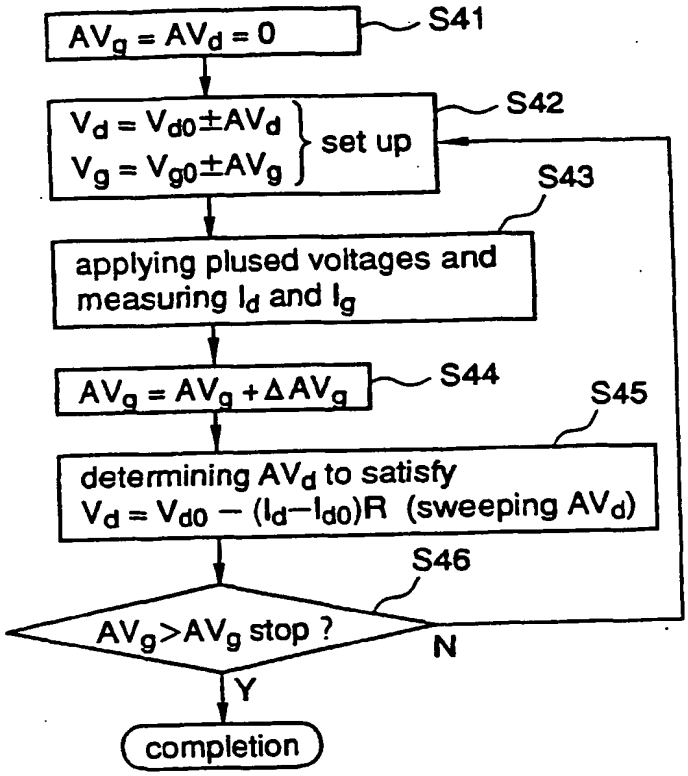
$AV_g = AV_d = 0$
S41
$V_d = V_{d0} \pm AV_d$
$V_g = V_{g0} \pm AV_g$
set up
S42
S43
applying plused voltages and measuring I_d and I_g
$AV_g = AV_g + \Delta AV_g$
S44
S45
determining AV_d to satisfy $V_d = V_{d0} - (I_d - I_{d0})R$ (sweeping AV_d)
S46
$AV_g > AV_g$ stop ?
N
Y
completion

Fig.29

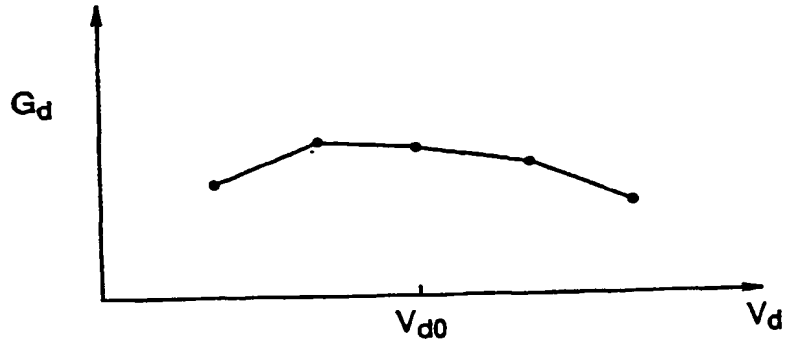
G_d
V_{d0}
V_d

Fig.30

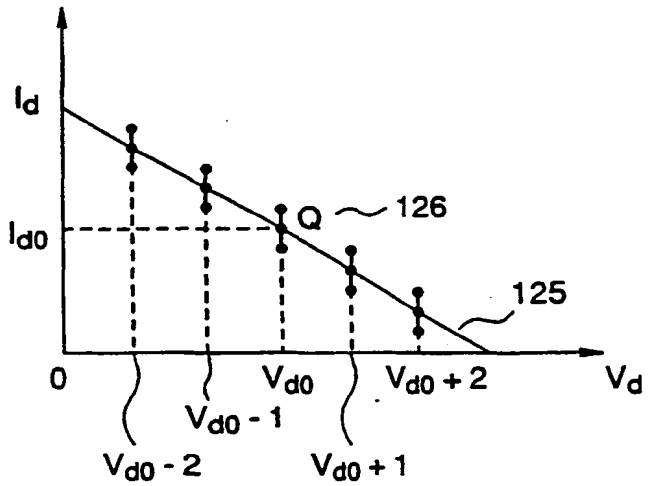

Fig.31

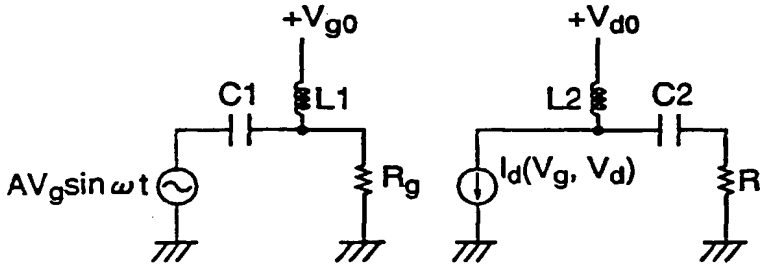

Fig.32

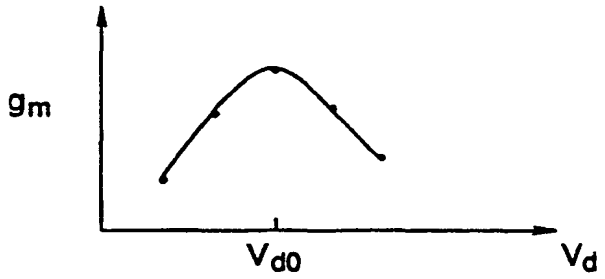

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Fig.33

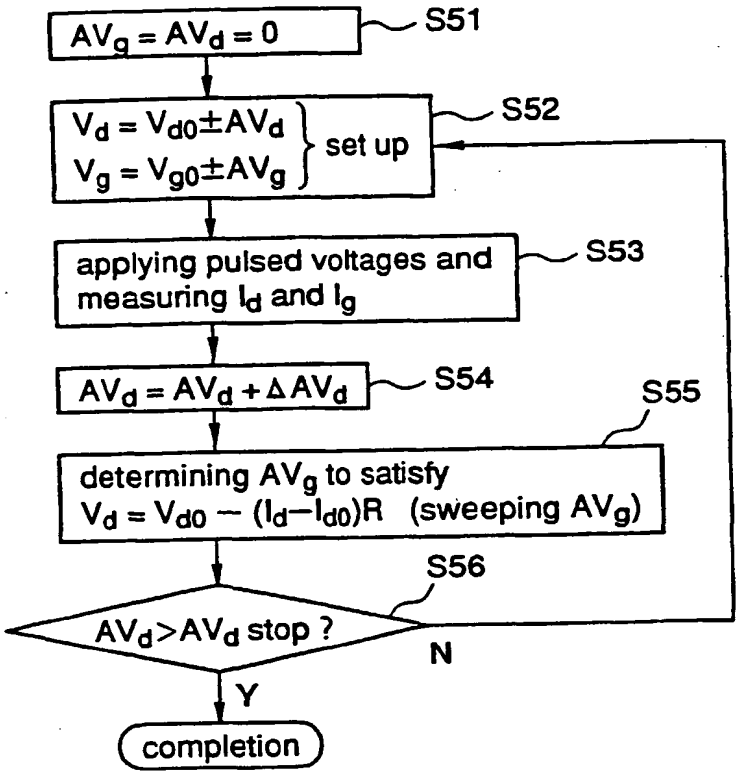

Fig.34

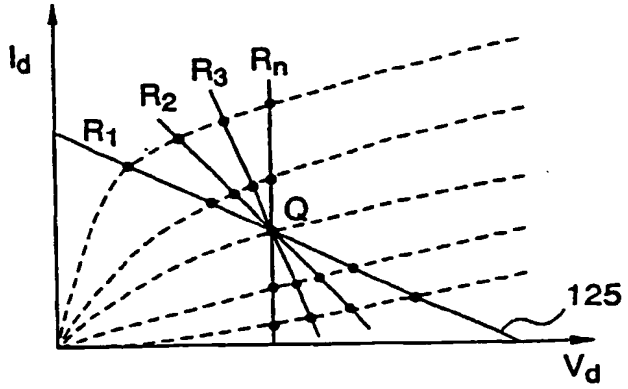

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Fig.35

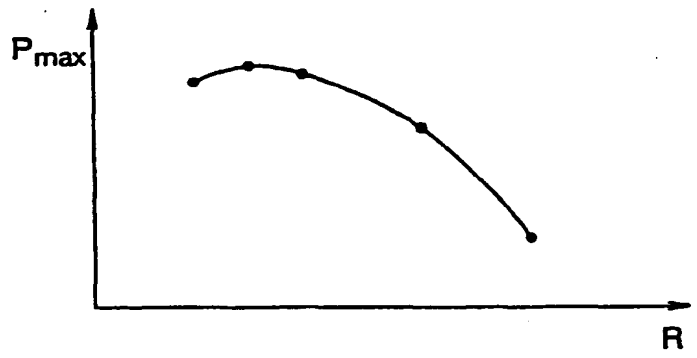
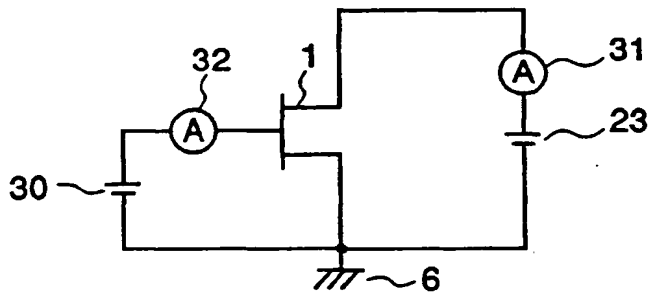


Fig.36 Prior Art



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(71) Applicant:
MITSUBISHI DENKI KABUSHIKI KAISHA
Tokyo 100 (JP)

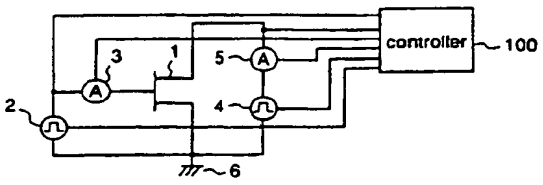
(72) Inventors:
- **Inoue, Akira**
  Chiyoda-ku, Tokyo 100 (JP)
- **Nakajima, Yasuharu**
  Chiyoda-ku, Tokyo 100 (JP)
- **Ohta, Yukio**
  Chiyoda-ku, Tokyo 100 (JP)
- **Matsubayashi, Hiroto**
  Chiyoda-ku, Tokyo 100 (JP)

(74) Representative:
KUHNEN, WACKER & PARTNER
Alois-Steinecker-Strasse 22
85354 Freising (DE)

(54) Apparatus and method for testing semiconductor element and semiconductor device

(57) An apparatus of testing a semiconductor element (Figs. 1 and 2) includes means for applying pulsed voltages being synchronized with each other, respectively, to a gate and a drain of a semiconductor element (1) as a target of testing, and means for measuring a current flowing through the semiconductor element (1) by the pulsed voltages thus applied. Therefore, it is provided an apparatus of testing a semiconductor element capable of obtaining the pulsed I-V characteristics with considerations of the influences of heat and surface level of a semiconductor element, and a RF swing along a load line in a large signal operation of a high-power output FET.

Fig.1



EP 0 800 091 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 10 0420

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	"narrow pulse measurement" ELECTRONICS LETTERS, vol. 23, no. 13, June 1987, HITCHIN, HERTS., GB, pages 686-687, XP002057571	1,2	G01R31/26
Y	* page 686, left-hand column, paragraph 3TH *	3-5	
Y	GRACIA ET AL.: "an optimized method" IEEE TRANS. ON INSTR. AND MEASUREMENT, vol. 37, no. 3, September 1988, NEW-YORK, US, pages 393-397, XP000096805 * figures 1,2 *	3,4	
Y	LESLIE B ET AL: "WAFER-LEVEL TESTING WITH A MEMBRANE PROBE" IEEE DESIGN & TEST OF COMPUTERS, vol. 6, no. 1, February 1989, pages 10-17, XP000027397 * page 10, paragraph 2 * * page 10, paragraph 2 - page 11, paragraph 2 * * figures 1,2 *	5	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G01R
A	"simple tester checks fet vp and gm" ELECTRONIC DESIGN, vol. 15, no. 10, May 1967, page 91 XP002057572 * page 91, right-hand column *	6-10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 July 1998	Lopez-Carrasco, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 97 10 0420

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 97 10 0420

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-4,6-10

   applying synchronized pulses

2. Claim : 5

   using membrane probe